**RPG- Retail Product Group**

**TLM – Test Launch Manager**

**FAR – Failure Analysis and Reproduction**

**SNAPSHOT**– We used this tool for VM (Virtual machine) administration.

**Firmware**: - Firmware is software that provides basic machine instructions that allow the hardware to function and communicate with other software running on a device.

* Manages the physical communication between the host and memory.
* Implements flash management algorithms to improve performance.

An interface between:

* The Front End (FE) – the host
* The Back End (BE) – the flash memory
* Manages the storing of data
* Combines physical structures into larger, meta-structures
* Attempts to keep active data in binary memory
* Manages Wear Levelling
* Manages Garbage Collection
* Reduces Write Amplification

**Flash Memory**:

* Flash memory is a long-life and non-volatile storage chip that is widely used in embedded systems.
* It can keep stored data and information even when the power is off. It can be electrically erased and reprogrammed.
* Flash memory was developed from EEPROM (electronically erasable programmable read-only memory).

**Flash storage devices**: All flash storage devices communicate with some sort of host.

* The host is a computer or any portable device like mobile phone or camera that provides services to storage devices.
* No matter what kind of medium is used, the host must use some form of File System to translate information to some location at storage.
* The file system as a piece of information is saved on the same storage device

**NAND**:

**What is SD card protocol?**

* SD Card protocol consists of an exchange of command and response between the host and the card. Data transfers occurs in packets.
* A packet consists of a data block and CRC check bits.
* Data transfer can occur in single block or multi block mode.

**CRC**-- A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to digital data.

**SATA protocol?**

Serial ATA (SATA) and Serial Attached SCSI (SAS) are data storage protocol standards that have the primary function of transferring data (directly or otherwise) between the host system and mass storage devices (e.g., hard disk drives, optical drives, and solid-state disks).

File handling in python,

Basics of C and Python

Oops concept

**BICS --** Bit Cost Scalable (BiCS) :

Bit Cost Scalable (BiCS) flash technology as a three-dimensional memory for the future ultra high density storage devices, which extremely reduces the chip costs by vertically stacking memory arrays.

Agile methodology …?

**What is a framework and example?** A framework is therefore a set of tools and modules that can be reused for various projects. One of the most well-known and used frameworks is the Microsoft . NET Framework for websites.

**Difference between Lambaeu and Felix ?**

**Lambaeu bics5x4 512 GB 2 Die(256GB ) Dies 4(512GB) Chip:- MMP0**

**Lambaeu bics5x4 1.5TB 12D 2Chip MMP4 one is dummy**

BiCS5 is the latest incarnation of 3D TLC NAND with up to 112 layers in a single NAND Flash chip. 3D NAND is where layers are stacked vertically rather than a single layer 2D NAND chip (SLC, MLC, pSLC). This had led to the incredibly fast development of 3D NAND Flash over the last 5 years.

A single cell is not much use–we need to combine multiple cells

To do this we use:

* **Bit lines**
* **Word lines §**
* **Pages**
* **Blocks**
* **Planes**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **BiCS 4** | **BiCS 5** | **BiCS 6** |
| Introduced | 2017 | 2020 | 2021 |
| Layers (Word lines) | 64 | 96 | 112 |

**X3** :- MLC Levels , Top level, middle level, lower level

It means MLC(Multi-Level-Cell) block is filled with SLC blocks, for example if we are dealing with x3 then capacity blocks should be filled with total 3 SLC(Single-Level-Cell) blocks only

**X4** :- MLC Levels , Upper level, Top level, middle level, lower level It means MLC(Multi-Level-Cell) block is filled with SLC blocks, for example if we are dealing with x4 then capacity blocks should be filled with total 4 SLC(Single-Level-Cell) blocks only.

SLC X1/D1 = 1 flash cell = 1 bit of information

MLC X2/D2 = 1 flash cell = 2 bits of information

MLC X3/D3 = 1 flash cell = 3 bits of information MLC X4/D4 = 1 flash cell = 4 bits of information

|  |  |  |
| --- | --- | --- |
| **Feature** | **SLC** | **MLC** |
| Transfer speeds | Fast | Slow |
| Power consumption | Low | High |
| Cell endurance | High | Low |
| Manufacturing cost per Mb | High | Low |
| Usage | High-performance memory cards where speed and reliability are important | Standard consumer memory devices |

**Folding:-**

And

Felix Bics5x3 128 GB ( 1D) F

elix bics6x3 256 GB (1D) (2D)

x3 and x4

why folding and direct write why we wrote data in different why not the same way

CTF and CVF me diff ye sb'

**1.     Package:-**

The physical unit that we use in commercial products

It consists of:

    At least one die (up to eight at the moment)

    All the pinout and wiring needed to connect it to the outside world

Dies can be stacked to increase capacity

**2.     Chip:-**

A chip can consist of one or more dies

Firmware controls addressing of dies through a “Chip Enable Line”

If two dies share the same Chip Enable Line they are part of the same chip

If two dies have different Chip Enable Lines they are separate chips

**3.     Die:-**

* A piece of a wafer that is composed of all the hardware components needed to work as a flash storage device
* Minimum independent NAND unit
* May be stacked into a single package (typically 1, 2, 4, 8, 16 die stacks)

**4.     Plane:-**

* Group of blocks
* Generally 1-4 per die
* May be programmed, read, or erased in parallel
* Is a physical unit on a die
* Has the ability to perform independently
* Exists to enable in-die interleaving
* Currently up to 8 planes on a die

**5.     Block:-**

* NAND architecture is based on independent blocks
* Blocks are the smallest erasable units
* A Block is the minimum unit for
  + ->Erasing

**6.     Page:-**

* The minimum flash unit for programming and reading
* Must be erased before programming, as charging cannot reduce a cell’s voltage
* Pages are the smallest programmable units
* Pages are still very small units – we combine multiple pages to form a Block
* A Page is the minimum unit for :-
* ->Programming
* 2->Reading
* A Block is the minimum unit for
  + ->Erasing

**7.     Word lines:-**A single cell can store very little data, so we combine a cells to create a word line

**8.     Cell(SLC/MLC):-**

* The cell may be treated as a capacitor, which has some voltage level on it
* The number of possible voltage levels in a cell determines the type of flash:

🡪**Single-Level Cell (SLC):-** SLC (D1 or X1) memory stores one bit of data in each cell

It takes two voltage levels to represent a single bit of data

🡪**Multi-Level Cell (MLC**):- MLC memory stores 2 or more bits of data in each cell

To represent 2 bits using a single cell (MLC D2/X2 memory), 4 voltage levels are needed:

**By combining one or more of the basic physical components we can define larger data structures**

* **Meta-pages**
* **Meta-blocks**
* **Meta-planes**

**NAND Operations:**

**🡪Erase 🡪Block Erase time ~5ms**

* The purpose of the flash memory erase operation:
* To move electrons from the floating gate back to the substrate, and
* Emptying the floating gate from any charge
* This is achieved by applying 20V to the substrate and using the tunneling phenomenon to empty the floating gate

**🡪Write 🡪Page Write Time <1msec**

* The purpose of the flash memory write operation:
* To move electrons into the floating gate.
* This is achieved by using a tunneling phenomenon (Fowler-Nordheim quantum-mechanical tunneling)
* By applying 20V to the gate voltage, electrons move from the silicon substrate into the floating gate

**🡪Read 🡪Page Read Time ~40-180 μsec**

* The purpose of the flash memory read operation is to distinguish between:
* A memory cell which has been programmed, and
* A memory cell which is erased
* By applying, for example, voltage = 3V, we are able to distinguish whether the cell is programmed or erased
* To sense the state of any one X3 cell, we need to apply multiple voltages to determine the cell’s charge.

**Controller:**

The Controller’s primary objectives:

* To translate an LBA to the address of memory cells on flash memory chip, thus providing “implementation” of Host’s read/write “interface”
* To control Host data integrity
* To optimize flash memory usage due to its wearing tendency

**For some applications (cameras, MP3 players), most data is moved straight onto long-term storage**

* These are relatively easy to handle
* Data can be moved from host directly into MLC
* Still need to do periodic read/scrub

**Other applications (mobile phones, flash-based operating systems) make frequent changes to data**

* Performance is improved if ‘active’ data is kept in SLC
* If data becomes ‘inactive’ it can be moved to MLC to make room in SLC

**Features:-**

**UM :- (Update Manager)**

* + Update Manager Routes host data according to size
  + For example we have 3 streams random, random intermediate and sequential
* **Random** usually have Meta data or very small text file
* **Random intermediate** images might be there
* **Sequential** means camera or video recording where we need to store more data in a single chunk

**FOLD:**

* Folding is the mechanism by which SLC data is moved into X3 MLC
* X3 blocks can be written only by the operation of folding (copying) an entire LG triplet from fully-written SLC blocks
* SLC to MLC (X3) folding is done by on-chip copy
* Blocks to be folded can contain:
* Data written by the host that is detected as ‘cold’
* Data that has aged in Update and Relocate blocks
* Data copied by compaction of MLC (X3) blocks

AT, AP, FILE50, GC, WA, PF, CONFIGPF, QLCWA, UECC, EPWR

**WA :- (Write abort)**

* Write abort means some power loss while programming to the nand, this is because of unwanted power loss or power failure.
* It occur when host requests for writes and in between power loss happens

**PF :- (Program failure)**

Program failure means while doing some programming or preforming write operation and in between some disturbance comes, that may be due to bad cells or factory defected cells. This failure will catch while we do EPWR for that  .